ABSTRACT OF THE DISCLOSURE

A semiconductor package utilizing insulating peripheral sealing portions and pattern leads and methods for manufacturing such semiconductor packages are provided. The semiconductor package includes a substrate on which a semiconductor chip is mounted. The substrate includes a plurality of substrate pads and the semiconductor chip includes a plurality of chip pads on an active surface. The semiconductor chip is surrounded by one or more peripheral sealing layers and conductive lead patterns are formed across the peripheral sealing layer(s) to connect the chip pads to corresponding substrate pads. The chip and lead patterns may be encapsulated and the substrate may also be provided with external connection structures such as solder balls to complete the package.